Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

M.E DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Second Semester

Applied Electronics

AP4001 – Applications Specific Integrated Circuits

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Define Semi-custom ASIC.	RE	1	2
2.	How transistors act as resistors.	RE	1	2
3.	Define Anti-fuse.	RE	2	2
4.	What are the blocks present in Xilinx I/O?	RE	2	2
5.	List the advantages of stratix FPGAs.	RE	3	2
6.	What are the signal probing techniques?	RE	3	2
7.	Define logic synthesis.	RE	4	2
8.	List the clocking strategies of ASIC.	RE	4	2
9.	What is high performance filter? Give example.	RE	5	2
10.	Outline the features of SDRAM.	UN	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Explain in detail about CMOS transistors with neat diagrams.	AP	1	13
		Or			
	b	Describe in detail about transistor parasitic capacitance and logical effort of ASIC.	AP	1	13
12.	a	Explain the following: EEPROM technology and Anti-fuse technology.	AP	2	13
		Or			
	b	With neat sketch, explain the xilinx 4000 CLB architecture.	AN	2	13
13.	a	Draw the architecture of cyclone and virtex and explain its configuration.	AP	3	13
		Or			
	b	Explain in detail about the nios based embedded systems.	AN	3	13
14.	a	Discuss in detail about floor planning of ASIC.	AP	4	13
		Or			
	b	Write about power and clocking strategies of ASIC.	AP	4	13

15.	a	Construct DAA and computation of FFT for high performance algorithm of ASIC.	AN	5	13
		Or			
	b	Analyze the case study of digital camera with relevant diagrams.	AN	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Explain in detail about Altera FLEX and altera MAX inputs and outputs with necessary diagrams.	UN	2	15
		Or			
	b	Explain the high speed standards used in ASICs.	UN	5	15